METHOD FOR CONTACT PAD ISOLATION

correction

Related Applications

[0001] This application is a divisional of U.S. App. Ser. No. 10/112,380, filed Mar. 28, 2002, which is now a U.S. Patent 6,638,144; which is a continuation of U.S. App. Ser. No. 09/467,667, filed Dec. 17, 1999 and issued as U.S. Pat. No. 6,396,300; which is a divisional of U.S. App. Ser. No. 09/023,639, filed Feb. 13, 1998 and issued as U.S. Pat. No. 6,114,878.

Technical Field

[0002] This invention relates generally to electronic devices and, more specifically, to a circuit and method for isolating a contact pad from a logic circuit.

Background of the Invention

[0003] Processed semiconductor wafers typically comprise an array of substantially isolated integrated circuitry locations, which are subsequently separated to form semiconductor dies. In order to test the operability of the integrated circuitry of a die location on a wafer, a wafer probe card is applied to each die location. The wafer probe card includes a series of pins that are placed in physical contact with a die location's contact pads, which in turn connect to the die location's circuitry. The pins apply voltages to the input contact pads and measure the resulting output electrical signals from the output contact pads. However, the wafer probe card's pins may not be able to extend to all of the contact pads. As a result, it is necessary to provide accessible redundant contact pads on the die location and couple them to particular logic circuits.

[0004] An additional hardware limitation relevant to testing the die locations is the spacing between the pins of the wafer probe card. Specifically, the pins may be